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[Abstract]

A semiconductor memory device is able to hide a refreshing operation without using a cache memory.

The refreshing operation is carried out based on a refresh signal generated within a semiconductor memory device, and data and parity data are stored together. When the semiconductor memory device refreshes data and reads data simultaneously, data of a memory cell which cannot be read because of the refreshing operation thereon is determined based on the parity data. When the semiconductor memory device refreshes data and writes data simultaneously, the data of a memory cell which cannot write data therein because of the refreshing operation thereon is temporarily stored and held in another memory area. The held data is subsequently written back in the original memory cell.

According to the present invention, when the semiconductor memory device refreshes data and reads or writes data simultaneously, the data of a memory cell which cannot be read is determined based on parity data, and the data of a memory which cannot write data therein is temporarily stored and held in another memory area. The held data is subsequently written back in the original memory cell. Therefore, the refreshing operation may be hidden without using a cache memory.